Distributed by:

JAMECO® ELECTRONICS

**www.Jameco.com ✦ 1-800-831-4242**

The content and copyrights of the attached material are the property of its owner.

Jameco Part Number 197114

# MC74HC02A

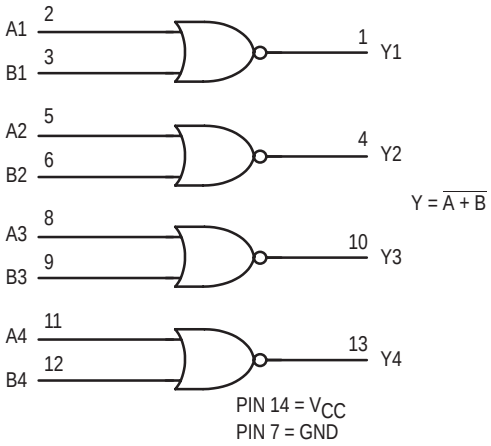
# Quad 2-Input NOR Gate

## High–Performance Silicon–Gate CMOS

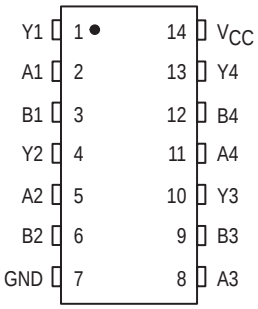
The MC74HC02A is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates

**LOGIC DIAGRAM**



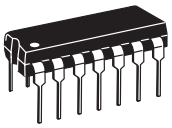

**PIN ASSIGNMENT**



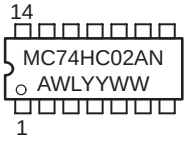

ON Semiconductor

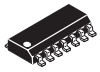
http://onsemi.com

**MARKING DIAGRAMS**

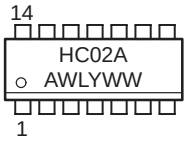


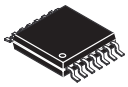
**PDIP–14**
**N SUFFIX**
**CASE 646**



**SOIC–14**
**D SUFFIX**
**CASE 751A**



**TSSOP–14**
**DT SUFFIX**
**CASE 948G**

A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

**FUNCTION TABLE**

| Inputs | | Output |
|---|---|---|
| **A** | **B** | **Y** |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MC74HC02AN | PDIP–14 | 2000 / Box |
| MC74HC02AD | SOIC–14 | 55 / Rail |
| MC74HC02ADR2 | SOIC–14 | 2500 / Reel |
| MC74HC02ADT | TSSOP–14 | 96 / Rail |
| MC74HC02ADTR2 | TSSOP–14 | 2500 / Reel |

© Semiconductor Components Industries, LLC, 2000

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | – 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | – 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP†<br>SOIC Package†<br>TSSOP Package† | 750<br>500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>Plastic DIP, SOIC or TSSOP Package | 260 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | – 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 1) $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>3.0<br>4.5<br>6.0 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | 1.5<br>2.1<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ – 0.1 V<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>3.0<br>4.5<br>6.0 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | 0.5<br>0.9<br>1.35<br>1.8 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{out}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$ $\|I_{out}\|$ ≤ 2.4 mA<br>$\|I_{out}\|$ ≤ 4.0 mA<br>$\|I_{out}\|$ ≤ 5.2 mA | 3.0<br>4.5<br>6.0 | 2.48<br>3.98<br>5.48 | 2.34<br>3.84<br>5.34 | 2.20<br>3.7<br>5.2 | |

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in} = V_{IH}$ or $V_{IL}$<br>$\|I_{out}\| \leq 20$ μA | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in} = V_{IH}$ or $V_{IL}$ $\|I_{out}\| \leq 2.4$ mA<br>$\|I_{out}\| \leq 4.0$ mA<br>$\|I_{out}\| \leq 5.2$ mA | 3.0<br>4.5<br>6.0 | 0.26<br>0.26<br>0.26 | 0.33<br>0.33<br>0.33 | 0.4<br>0.4<br>0.4 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in} = V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$\|I_{out}\| = 0$ μA | 6.0 | 1.0 | 10 | 40 | μA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

**AC ELECTRICAL CHARACTERISTICS** ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | – 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>30<br>15<br>13 | 95<br>40<br>19<br>16 | 110<br>55<br>22<br>19 | ns |
| $t_{TLH}$,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 1 and 2) | 2.0<br>3.0<br>4.5<br>6.0 | 75<br>30<br>15<br>13 | 95<br>40<br>19<br>16 | 110<br>55<br>22<br>19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC} = 5.0$ V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Gate)* | 22 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

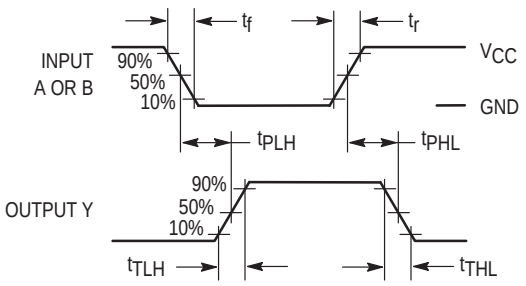
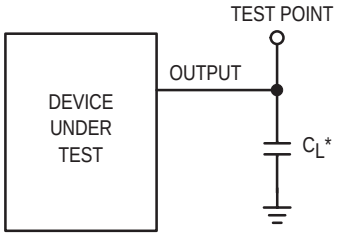


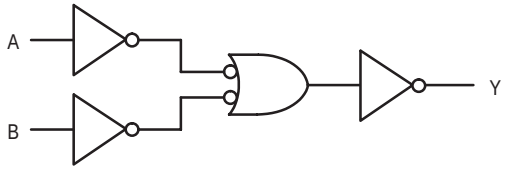

**Figure 1. Switching Waveforms**




*Includes all probe and jig capacitance

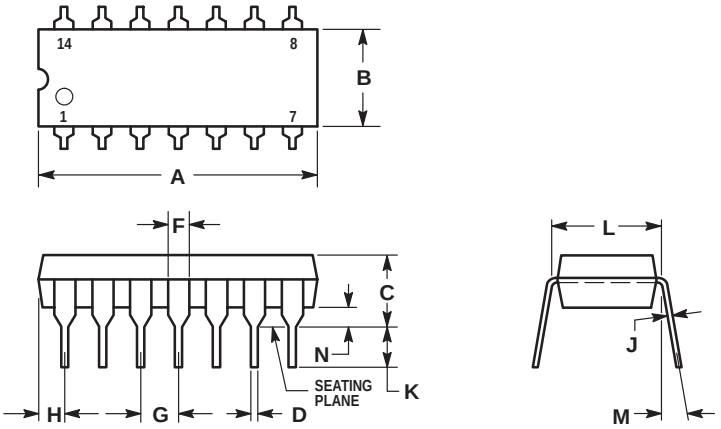
**Figure 2. Test Circuit**

**EXPANDED LOGIC DIAGRAM**
**(1/4 OF THE DEVICE)**



## PACKAGE DIMENSIONS

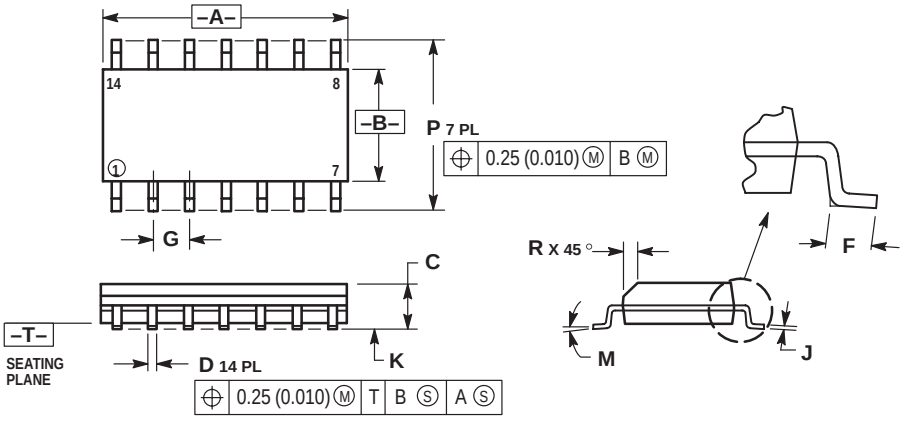
**PDIP–14**
**N SUFFIX**
CASE 646–06
ISSUE L




NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.715 | 0.770 | 18.16 | 19.56 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.145 | 0.185 | 3.69 | 4.69 |
| D | 0.015 | 0.021 | 0.38 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.78 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.052 | 0.095 | 1.32 | 2.41 |
| J | 0.008 | 0.015 | 0.20 | 0.38 |
| K | 0.115 | 0.135 | 2.92 | 3.43 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 10° | 0° | 10° |
| N | 0.015 | 0.039 | 0.39 | 1.01 |

**SOIC–14**
**D SUFFIX**
CASE 751A–03
ISSUE F

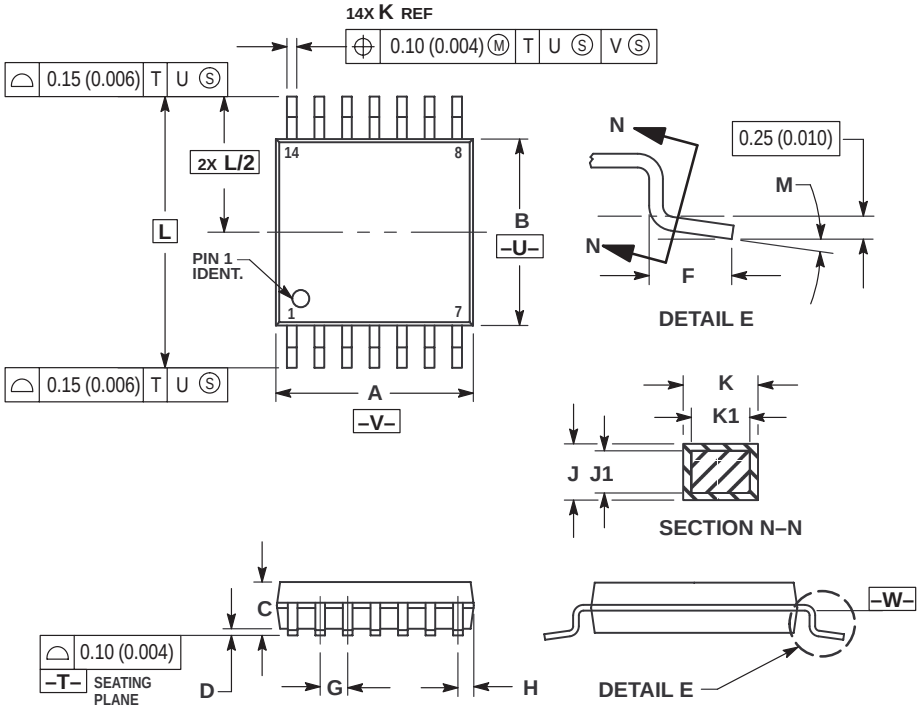



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 8.55 | 8.75 | 0.337 | 0.344 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.228 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

## PACKAGE DIMENSIONS

**TSSOP–14**
**DT SUFFIX**
CASE 948G–01
ISSUE O




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

# Notes

**ON Semiconductor** and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

**NORTH AMERICA Literature Fulfillment**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
**Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
**Email**: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

**N. American Technical Support**: 800–282–9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support
**German Phone**: (+1) 303–308–7140 (M–F 1:00pm to 5:00pm Munich Time)
**Email**: ONlit–german@hibbertco.com
**French Phone**: (+1) 303–308–7141 (M–F 1:00pm to 5:00pm Toulouse Time)
**Email**: ONlit–french@hibbertco.com
**English Phone**: (+1) 303–308–7142 (M–F 12:00pm to 5:00pm UK Time)
**Email**: ONlit@hibbertco.com

**EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781**
*Available from Germany, France, Italy, England, Ireland

**CENTRAL/SOUTH AMERICA:**
**Spanish Phone**: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
**Email**: ONlit–spanish@hibbertco.com

**ASIA/PACIFIC**: LDC for ON Semiconductor – Asia Support
**Phone**: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
**001–800–4422–3781**
**Email**: ONlit–asia@hibbertco.com

**JAPAN**: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–8549
**Phone**: 81–3–5740–2745
**Email**: r14525@onsemi.com

**ON Semiconductor Website**: http://onsemi.com

For additional information, please contact your local
Sales Representative.